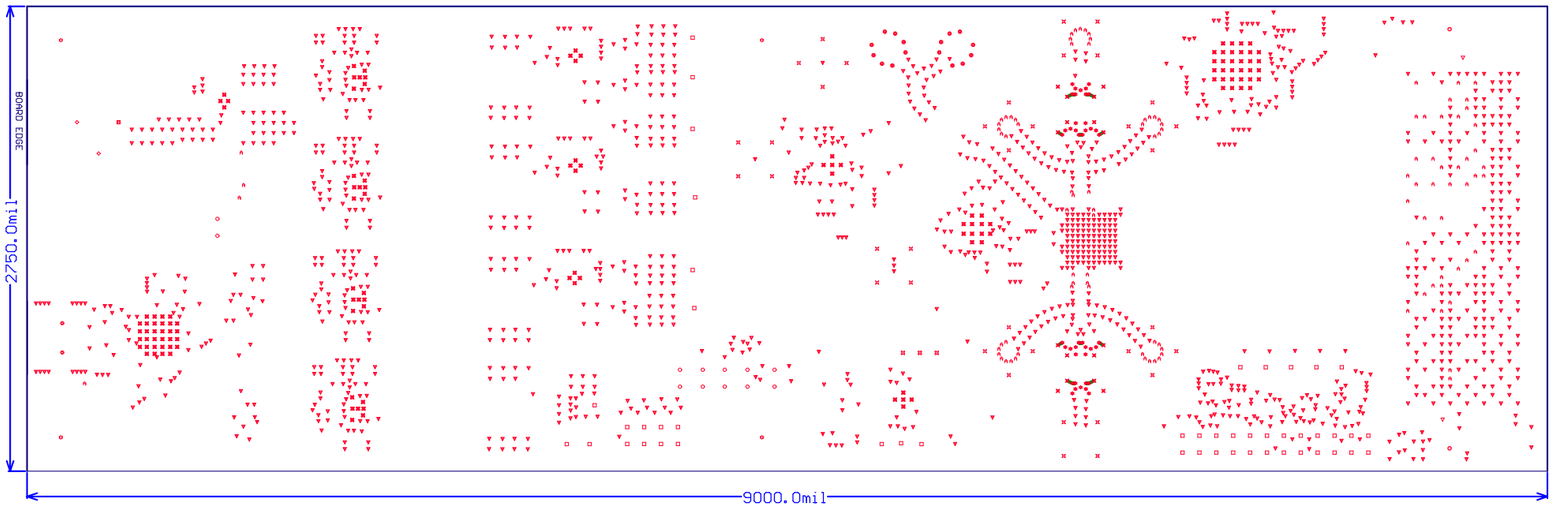
1.ALL 11.5 MIL TRACES ON L01 LAYER NEED TO BE HAVE 50 OHM IMPEDANCE +/- 10%
2.ALL 11.5 MIL TRACES ON L14 LAYER NEED TO BE HAVE 50 OHM IMPEDANCE +/- 10%
3.ALL 3.3 MIL TRACES ON L03 AND L12 LAYER NEED TO BE HAVE 50 OHM IMPEDANCE +/- 10%
4.ALL 7 MIL TRACE WIDTH WITH 7 MIL AIRGAP ON L01 AND L14 LAYERS NEED TO BE HAVE 100 OHM TIGHTLY COUPLED DIFFERENTAIL IMPEDANCE +/- 10%
5.ALL 10.5 MIL TRACE WIDTH WITH 20.5 MIL AIRGAP ON L01 AND L14 LAYERS NEED TO BE HAVE 100 OHM DIFFERENTAIL IMPEDANCE +/- 10%
6.ALL 3.25 MIL TRACE WIDTH WITH 8 MIL AIRGAP ON L03 AND L12 LAYERS NEED TO BE HAVE 100 OHM DIFFERENTAIL IMPEDANCE +/- 10%
7.NO VENDOR LOGO OR NAME ON THE BOARD
8.HOLES LESS THAN 12 MIL ARE DRILL SIZES AND NOT FINISHED HOLE SIZES (FHS)
9.MINIMUM PLATING IN ALL THE THROUGH HOLE SHALL BE 0.001 INCH Cu
10.ALL 8.00 MIL VIAS SHOULD BE NON CONDUCTIVE VIA FILLING FROM TOP AND BOTTOM SIDE

12. ALL THROUGH VIAS TO BE PLUGGED WITH NON-CONDUCTIVE EPOXY. PLUGGED VIAS TO BE PLATED OVER TO PRESENT FLAT SURFACE. NO POTHOLES.

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type	Physical Length	Rout Path Length
▣	1	39.76mil (1.010mm)	PTH	Slot	140.16mil (3.560mm)	100.39mil (2.550mm)
◇	2	29.92mil (0.760mm)	PTH	Slot	120.08mil (3.050mm)	90.16mil (2.290mm)
◎	2	35.43mil (0.900mm)	NPTH	Round	-	-
▽	2	50.00mil (1.270mm)	NPTH	Round	-	-
✣	2	106.00mil (2.692mm)	NPTH	Round	-	-
⊠	3	45.28mil (1.150mm)	PTH	Round	-	-
☼	4	125.98mil (3.200mm)	PTH	Round	-	-
○	12	40.16mil (1.020mm)	PTH	Round	-	-
⊞	16	15.75mil (0.400mm)	PTH	Round	-	-
✖	16	25.00mil (0.635mm)	PTH	Round	-	-
⌑	36	59.06mil (1.500mm)	PTH	Round	-	-
✲	42	10.00mil (0.254mm)	PTH	Round	-	-
□	49	40.00mil (1.016mm)	PTH	Round	-	-
⍓	102	8.00mil (0.203mm)	PTH	Round	-	-
✖	130	7.87mil (0.200mm)	PTH	Round	-	-
▽	1486	8.00mil (0.203mm)	PTH	Round	-	-
	1905 Total					

Slot definitions : Rout Path Length = Calculated from tool start centre position to tool end centre position.
Physical Length = Rout Path Length + Tool Size = Slot length as defined in the PCB layout

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top SilkScreen				
	Top Solder Mask	TAIYO-4000-BN	0.50mil	3.9	
1	Top Copper	Copper	2.00mil		COPPER +PLATING
	Dielectric 1	MEG6-R-5775K	6.00mil	3.42	
2	Layer 2 (GND1)	Copper	0.60mil		
	Dielectric 2	MEG6-R-5670K	3.30mil	3.23	
3	Layer 3 (SIG1)	Copper	0.60mil		
	Dielectric 3	MEG6-R-5775K	3.00mil	3.42	
4	Layer 4 (GND2	Copper	0.60mil		
	Dielectric 4	MEG6-R-5670K	3.50mil	3.23	
5	Layer 5 (PWR1)	Copper	1.20mil		
	Dielectric 5	MEG6-R-5775K	2.60mil	3.58	
6	Layer 6 (GND3)	Copper	1.20mil		
	Dielectric 6	MEG6-R-5670K	3.00mil	3.23	
7	Layer 7 (PWR/SIGNAL2)	Copper	1.20mil		
	Dielectric 7	MEG6-R-5775K	3.00mil	3.42	
8	Layer 8 (PWR/SIGNAL3)	Copper	1.20mil		
	Dielectric 8	MEG6-R-5670K	3.00mil	3.23	
9	Layer 9 (GND4)	Copper	1.20mil		
	Dielectric 9	MEG6-R-5775K	2.60mil	3.58	
10	Layer 10 PWR2)	Copper	1.20mil		
	Dielectric 10	MEG6-R-5670K	3.50mil	3.23	
11	Layer 11 (GND5)	Copper	0.60mil		
	Dielectric 11	MEG6-R-5775K	3.00mil	3.42	
12	Layer 12 (SIG4)	Copper	0.60mil		
	Dielectric 12	MEG6-R-5670K	3.30mil	3.23	
13	Layer 13 (GND6)	Copper	0.60mil		
	Dielectric 13	MEG6-R-5775K	6.00mil	3.42	
14	Bottom Copper	Copper	2.00mil		COPPER + PLATING
	Bottom Solder Mask	TAIYO-4000-BN	0.50mil	3.9	
	Bottom Silk				



M10 Fab Notes

DESIGN INFORMATION

MIN. TRACK WIDTH: 3.25 MIL
MIN. CLEARANCE: 4 MIL
MIN. VIA PAD SIZE: 15.7 MIL
MINIMUM ANNULAR RING 5mil EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER TAIYO 4000/MEG6
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH MIN COPPER THICKNESS: [X] 1MIL [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR:
[ ] GREEN [ ] BLUE [X] OTHER RED
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER MECH LAYER 1
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] UL 94V-0 [X] RoHS [ ] OTHER PER ORDER
ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
MANUFACTURER'S UL: [ ] RAIL [ ] METAL [X] SILK

TEXAS INSTRUMENTS

PROJECT TITLE: ADC12DJ5200RF EVM
DESIGNED FOR: TI
FILE NAME: ADC12DJ5200RF EVM

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: N/A / REV: D / SVN REV: Not In VersionControl
LAYER NAME = Drill Drawing	M2 Board Dimensions
PLOT NAME = Fabrication Drawing	GENERATED : 27-Mar-21 6:15:38 AM / TEXAS INSTRUMENTS

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

ENGINEER: DWG	LAYOUT BY: BMR
print_Scale: 1:1	ALTIUM DESIGNER VERSION: 305-PD18-0843